UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,180	02/19/2002	Neil G. Morrow	TI-31574	5454

23494 7590 04/29/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	3

DATE MAILED: 04/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,180	MORROW, NEIL G.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *12 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification and drawings do not describe the host bus being an LPC bus as defined by Intel 1997.

3. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification and drawings do not describe the serial link being an AC Link or an LPC Link.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5, 8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,802,324 to Wunderlich et al. ("Wunderlich") and US Patent Number 6,070,214 to Ahern ("Ahern").

6. In reference to Claim 1, Wunderlich teaches a system for extending a signal path of a host bus comprising: a first repeater portion connected to a first segment of the host bus (See Figure 2 Numbers 112 and 200 and Column 5 Lines 47-48); a second repeater portion connected to a second segment of the host bus (See Figure 2 Numbers 118 and 202 and Column 5 Lines 49-50). Wunderlich does not teach that the first and second portions of the repeater are connected by a serial link and that the second portion is located remote from the first portion of the host bus. Ahern teaches using a serial link to connect two remotely located bus interfaces (See Figure 2 Number 40,46, Figure 5 Number 40,46, Column 7 Lines 21-33, and Column 9 Lines 19-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the repeater of Wunderlich with the serial link allowing

the interfaces to be remotely located of Ahern, resulting in the invention of Claim 1, in order to allow the bus repeater, which requires minimal configuration (See Column 2 Line 36 – Column 3 Line 18 of Wunderlich), to extend a bus from a portable computer to a docking station without having to connect all of the bus lines between the portable computer and docking station, and thus eliminate the need for a large cable with high latency (See Column 2 Lines 18-22 of Ahern).

7. In reference to Claim 5, Wunderlich and Ahern teach the limitations as applied to Claim 1 above. Wunderlich further teaches an interface to the host bus segment (See Figure 2 and Column 5 Lines 46-50). Ahern further teaches an interface to the host bus segment (See Figure 1 Number 14 and Column 5 Line 66 – Column 6 Line 3); a transaction queue with a data buffer connected to the interface (See Figure 1 Number 18 and Column 6 Lines 9-24); and a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link (See Figure 1 Number 38 and Column 6 Lines 40-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the repeater of Wunderlich with the serial link allowing the interfaces to be remotely located of Ahern, resulting in the invention of Claim 5, in order to allow the bus repeater, which requires minimal configuration (See Column 2 Line 36 – Column 3 Line 18 of Wunderlich), to extend a bus from a portable computer to a docking station without having to connect all of the bus lines between the portable

computer and docking station, and thus eliminate the need for a large cable with high latency (See Column 2 Lines 18-22 of Ahern).

8. In reference to Claim 8, Wunderlich, and Ahern teach the limitations as applied to Claim 5 above. Ahern further teaches a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link (See Figure 1 Number 26, Column 6 Lines 40-46, and Column 7 Lines 7-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the repeater of Wunderlich with the serial link allowing the interfaces to be remotely located of Ahern, resulting in the invention of Claim 8, in order to allow the bus repeater, which requires minimal configuration (See Column 2 Line 36 – Column 3 Line 18 of Wunderlich), to extend a bus from a portable computer to a docking station without having to connect all of the bus lines between the portable computer and docking station, and thus eliminate the need for a large cable with high latency (See Column 2 Lines 18-22 of Ahern).

9. In reference to Claim 11, Wunderlich teaches a bus repeater circuit having an interface to a host bus segment (See Figure 2 and Column 5 Lines 46-50). Wunderlich does not teach a transaction queue with a data buffer connected to the interface; a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over an external serial link. Ahern

teaches an interface to a host bus segment (See Figure 1 Number 14 and Column 5 Line 66 – Column 6 Line 3); a transaction queue with a data buffer connected to the interface (See Figure 1 Number 18 and Column 6 Lines 9-24); and a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link (See Figure 1 Number 38 and Column 6 Lines 40-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the repeater of Wunderlich with the serial link allowing the interfaces to be remotely located of Ahern, resulting in the invention of Claim 11, in order to allow the bus repeater, which requires minimal configuration (See Column 2 Line 36 – Column 3 Line 18 of Wunderlich), to extend a bus from a portable computer to a docking station without having to connect all of the bus lines between the portable computer and docking station, and thus eliminate the need for a large cable with high latency (See Column 2 Lines 18-22 of Ahern).

10. Claims 2, 3, 6, 7, 9, 10, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wunderlich and Ahern as applied to Claim 1 above, and further in view of The Free On-Line Dictionary of Computing ("FOLDOC").

11. In reference to Claim 2, Wunderlich and Ahern teach the limitations as applied to Claim 1 above. Wunderlich and Ahern do not teach that the serial link is chosen from one of the following: LVDS, Gigabit Ethernet, InfiniBand, IEEE1394, RF Wireless,

Infrared Wireless, or any combination of these. FOLDOC teaches the use of an IEEE-1394 serial link (See entry 'High Performance Serial Bus').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich and Ahern with the IEEE-1394 serial link of FOLDOC, resulting in the invention of Claim 2, because IEEE-1394 offers high-speed communications at speeds of 100, 200, or 400 Mbps, isochronous real-time data services, peer to peer communication, and a convenient six wire cable; and because it has a possible application to home automation using repeaters (See entry 'High Performance Serial Bus' in FOLDOC).

12. In reference to Claim 3, Wunderlich, Ahern, and FOLDOC teach the limitations as applied to Claim 2 above. Wunderlich further teaches that the host bus is a PCI bus (See Figure 2 Numbers 112 and 118 and Column 5 Lines 21-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich and Ahern with the IEEE-1394 serial link of FOLDOC, resulting in the invention of Claim 3, because IEEE-1394 offers high-speed communications at speeds of 100, 200, or 400 Mbps, isochronous real-time data services, peer to peer communication, and a convenient six wire cable; and because it has a possible application to home automation using repeaters (See entry 'High Performance Serial Bus' in FOLDOC).

13. In reference to Claim 6, Wunderlich, Ahern, and FOLDOC teach the limitations as applied to Claim 3 above. Wunderlich further teaches an interface to the host bus segment (See Figure 2 and Column 5 Lines 46-50). Ahern further teaches an interface to the host bus segment (See Figure 1 Number 14 and Column 5 Line 66 – Column 6 Line 3); a transaction queue with a data buffer connected to the interface (See Figure 1 Number 18 and Column 6 Lines 9-24); and a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link (See Figure 1 Number 38 and Column 6 Lines 40-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich and Ahern with the IEEE-1394 serial link of FOLDOC, resulting in the invention of Claim 6, because IEEE-1394 offers high-speed communications at speeds of 100, 200, or 400 Mbps, isochronous real-time data services, peer to peer communication, and a convenient six wire cable; and because it has a possible application to home automation using repeaters (See entry 'High Performance Serial Bus' in FOLDOC).

14. In reference to Claim 7, Wunderlich, Ahern, and FOLDOC teach the limitations as applied to Claim 2 above. Wunderlich further teaches an interface to the host bus segment (See Figure 2 and Column 5 Lines 46-50). Ahern further teaches an interface to the host bus segment (See Figure 1 Number 14 and Column 5 Line 66 – Column 6 Line 3); a transaction queue with a data buffer connected to the interface (See Figure 1

Number 18 and Column 6 Lines 9-24); and a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link (See Figure 1 Number 38 and Column 6 Lines 40-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich and Ahern with the IEEE-1394 serial link of FOLDOC, resulting in the invention of Claim 7, because IEEE-1394 offers high-speed communications at speeds of 100, 200, or 400 Mbps, isochronous real-time data services, peer to peer communication, and a convenient six wire cable; and because it has a possible application to home automation using repeaters (See entry 'High Performance Serial Bus' in FOLDOC).

15. In reference to Claim 9, Wunderlich, Ahern, and FOLDOC teach the limitations as applied to Claim 6 above. Ahern further teaches a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link (See Figure 1 Number 26, Column 6 Lines 40-46, and Column 7 Lines 7-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich and Ahern with the IEEE-1394 serial link of FOLDOC, resulting in the invention of Claim 9, because IEEE-1394 offers high-speed communications at speeds of 100, 200, or 400 Mbps, isochronous real-time data services, peer to peer communication, and a convenient six wire cable; and

because it has a possible application to home automation using repeaters (See entry 'High Performance Serial Bus' in FOLDOC).

16. In reference to Claim 10, Wunderlich, Ahern, and FOLDOC teach the limitations as applied to Claim 7 above. Ahern further teaches a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link (See Figure 1 Number 26, Column 6 Lines 40-46, and Column 7 Lines 7-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich and Ahern with the IEEE-1394 serial link of FOLDOC, resulting in the invention of Claim 10, because IEEE-1394 offers high-speed communications at speeds of 100, 200, or 400 Mbps, isochronous real-time data services, peer to peer communication, and a convenient six wire cable; and because it has a possible application to home automation using repeaters (See entry 'High Performance Serial Bus' in FOLDOC).

17. In reference to Claim 12, Wunderlich, Ahern, and FOLDOC teach the limitations as applied to Claim 9 above. As in Claim 9, Ahern teaches a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link (See Figure 1 Number 26, Column 6 Lines 40-46, and Column 7 Lines 7-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich and Ahern with the IEEE-1394 serial link of FOLDOC, resulting in the invention of Claim 12, because IEEE-1394 offers high-speed communications at speeds of 100, 200, or 400 Mbps, isochronous real-time data services, peer to peer communication, and a convenient six wire cable; and because it has a possible application to home automation using repeaters (See entry 'High Performance Serial Bus' in FOLDOC).

18. In reference to Claim 14, Wunderlich, Ahern, and FOLDOC teach the limitations as applied to Claim 12 above. As in Claim 3, from which Claim 14 depends, Wunderlich teaches that the host bus is a PCI bus (See Figure 2 Numbers 112 and 118 and Column 5 Lines 21-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich and Ahern with the IEEE-1394 serial link of FOLDOC, resulting in the invention of Claim 14, because IEEE-1394 offers high-speed communications at speeds of 100, 200, or 400 Mbps, isochronous real-time data services, peer to peer communication, and a convenient six wire cable; and because it has a possible application to home automation using repeaters (See entry 'High Performance Serial Bus' in FOLDOC).

19. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wunderlich, Ahern, and FOLDOC as applied to Claim 2 above, and further in view of The Low Pin Count (LPC) Interface Specification from Intel ("Intel-LPC").

20. In reference to Claim 4, Wunderlich, Ahern, and FOLDOC teach the limitations as applied to Claim 2 above. Wunderlich, Ahern, and FOLDOC do not teach that the host bus is an LPC (Low Pin Count) bus as defined by Intel 1997. Intel-LPC teaches the use of a Low Pin Count bus (See Page 1 Chapter 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich, Ahern, and FOLDOC with the Low Pin Count bus of Intel-LPC, resulting in the invention of Claim 4, because LPC has a reduced cost, allows synchronous design, is transparent and thus does not require special drivers or configuration, and supports desktop and mobile implementations (See Page 1 Section 1.1 of Intel-LPC).

21. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wunderlich and Ahern as applied to Claim 11 above, and further in view of Texas Instruments Application Report "Time Budgeting of the Flatlink™ Interface" ("TI-Flatlink").

22. In reference to Claim 13, Wunderlich and Ahern teach the limitations as applied to Claim 11 above. Wunderlich and Ahern do not teach that the serial link is chosen

from one of the following: LVDS(Flatlink), AC Link, LPC link. TI-Flatlink teaches the use of a Flatlink interface (See TI-Flatlink).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Wunderlich, Ahern, and FOLDOC with the Flatlink interface of TI-Flatlink, resulting in the invention of Claim 13, because Flatlink provides a point-to-point data transmission interface that provides better than a two-to-one reduction in the number of signal lines with no loss of data throughput (See Introduction of TI-Flatlink).

Claim Objections

23. Claim 12 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 12 reads "The repeater according to claim 9, further comprising a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link." Claim 9 reads "The system according to claim 6, further comprising a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link." As Claim 1 indicates that the system is a repeater, Claim 12 does not constitute a further limitation over Claim 9.

24. Claim 14 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 14 reads "The repeater according to claim 12, wherein the host bus is a PCI bus." Claim 12 is dependent from Claim 9, which is dependent on Claim 6, which is dependent on Claim 3 which reads "The system according to claim 2, wherein the host bus is a PC bus." As Claim 1 indicates that the system is a repeater, Claim 14 does not constitute a further limitation over Claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

tjc

Thomas J. Cleary
Patent Examiner
Art Unit 2111